(19) Europäisches Patentamt
European Patent Offic
Office européen des br vets

(11) EP 0 811 850 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
10.12.1997 Bulletin 1997/50

(51) Int Cl.[6]: **G01R 31/30**, G06F 1/28

(21) Application number: **97870078.9**

(22) Date of filing: **29.05.1997**

(84) Designated Contracting States:
AT BE DE ES FI FR GB IT NL SE

(30) Priority: **05.06.1996 US 19357 P**

(71) Applicants:
- **INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM VZW**
  3001 Heverlee (BE)
- **Katholieke Hogeschool Brugge-Oostende Vereniging Zonder Winstbejag**
  8000 Brugge (BE)

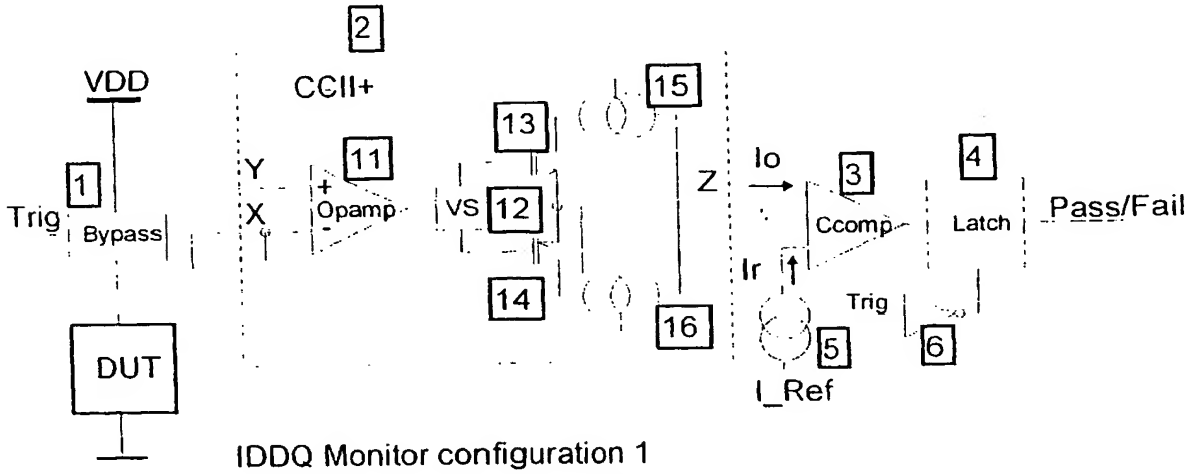
(72) Inventors:
- **Manhaeve, Hans**
  8200 Sint Michels (Brugge) (BE)
- **Kerckenaere, Stefaan**
  8480 Eernegem (BE)
- **Stopjakova, Viera**
  02962 Oravske Vesele (SK)

(74) Representative: **Van Malderen, Joelle et al**
Office Van Malderen,
Place Reine Fabiola 6/1
1083 Bruxelles (BE)

(54) High resolution supply current test system

(57) The present invention relates to a system for the measurement of a supply current of an electronic circuit, comprising:

a first part with control means for applying and controlling at least one voltage and one current on said circuit;
a second part being fed by an input voltage and delivering a first output voltage and a first output current on a first terminal and a second output current on a second terminal, said first output voltage being essentially equal to said input voltage, said second output current being essentially proportional to said first output current being said supply current;
a switch in between said first and said second part, being controlled by trigger means controlled by said first part, for turning said switch off or on whereby switching said second part in measurement mode or in bypass mode.



IDDQ Monitor configuration 1

Figure 1.

EP 0 811 850 A2

Description

Field of the invention

The present invention relates to a system for the measurement of the supply current of an electronic device or of an integrated circuit. More in particular a system for supply current testing of an electronic device or integrated circuit is disclosed.

Background of the Invention

It has been proven that quiescent supply current (I_{DDQ}) monitoring is a suitable test technique which can be used as well for the verification of electronic devices or circuits as well as to increase the test quality of said devices or circuits. Especially in function of improved test quality an accurate supply current measurement system is needed.

Among functional, stuck-at, stuck-open, and Quiescent current test strategies, no single test method guarantees detection of all types of defects in electronic devices. As types of defects in electronic devices, a number of defects occurring in digital CMOS devices can be mentioned, such as gate-oxide shorts, bridges and floating gates. Such defects are not detected by a conventional voltage based test approach. Many defects that pose reliability risks are detected only by I_{DDQ} testing, therefore multiple and accurate I_{DDQ} tests are necessary for CMOS devices or IC's. The I_{DDQ} test is the most sensitive and comprehensive strategy, but is a relatively slow measurement technique. The Quiescent current testing technique is based upon the fact that defective devices produce an abnormally high value of power supply current (I_{DD}). The technique has been proven to be very efficient in detecting certain defects occurring in CMOS devices or IC's, requiring only a reduced number of test patterns.

The overall test cost of a circuit depends on the test pattern generation time, the fault coverage required, tester time for each unit of the circuit, and the number of circuits under test. While current test generation takes much less CPU time and generates fewer test patterns, testing a circuit using current tests (applied at kHz rates) requires more time than using logic tests (applied at MHz rates). Measuring the I_{DDQ} current off-chip using a test monitor that is not on one chip with the electronic circuit or device that is tested causes difficulties for testing hardware and significantly decreases the test rate if standard measurement equipment, such as the Parametric Measurement Unit (PMU), is used. Basically two solutions to this problem exist. Using an on-chip monitor, integrated on one chip with the integrated circuit that is tested, can increase the test rate significantly. The alternative is to use a dedicated off-chip monitor. Nevertheless most I_{DDQ} measurements in production testing nowadays are still done with off-chip instrumentation. A few experimental on-chip/off-chip current monitors have been proposed so far. One of them is already used in production testing.

To be able to perform I_{DDQ} testing in an economical justified way, a dedicated measurement unit is needed. As on-chip built-in current monitors can achieve much higher testing speeds than off-chip alternatives, they have been evaluated as an appropriate choice for CMOS VLSI current testing.

Problem Definition

To measure accurately the quiescent supply current of the electronic circuit or Device Under Test (DUT), the measuring device should not influence the DUT's supply voltage and current in any condition, and be capable of driving the parasitic capacitance resulting from the DUT's supply wiring and decoupling capacitance. Most of the Built-in current monitors (BICs) presented so far are either intended to be inserted into the ground connection or leave the DUT's supply floating during measuring. By inserting a measuring device in the ground connection, a virtual ground for the devices under test is created, which when a current is flowing differs from the actual ground and thus affects the measurement accuracy.

The use of the Parametric Measurement Unit (PMU) available on a test system in a force voltage measure current mode offers a quantitative and accurate measurement. However the PMU is rather slow - measurement periods typically being 100 ms - and is not able to deliver switching spikes greater than 100 mA. As an example of such a device the PMU available on the Credence VISTAvision test system can be taken.

A monitor circuit called IDUNA, and disclosed in EP-0386804 was originally designed to serve as an on-chip monitor but can also be used as an off-chip monitor. The IDUNA generates a pass/fail decision based on an integrated comparison of the I_{DDQ} against a scaled reference current. The advantage of the circuit is that its possible to reach high measuring speeds, improved accuracy and noise immunity. The monitor is designed to operate at frequencies above 1 MHz. Despite its advantages however, the IDUNA is not capable of driving high capacitive loads. It cannot deliver high transient currents and requires a complex characterisation and calibration procedure as its measurement characteristic is non linear. The IDUNA is intended to perform an accurate comparison of the measured quiescent current against a predefined reference current level rather than to perform an accurate current measurement of the

quiescent current within a certain measurement range. Furthermore, due to its limited current delivering capability and limited capacitive load driving capability the IDUNA can only be used to test small circuits, and requires circuit partitioning in combination with the use of multiple monitors when on-chip current monitoring of bigger circuits is desired.

The OCIMU circuit, as disclosed in EP-0672911 is an off-chip monitor that is realised using discrete components. The OCIMU is capable of performing a relativ ly high speed (measurement time about 100 µs for a 2 µF load) current measurement especially when driving a high capacitive load (up to several µF). This property is important as modern complex ASICs usually have multiple supply pins (sometimes more than 20). To assure a high quality stable supply on the chip a 100 nF decoupling capacitance is added to each of these supply pins. So a total decoupling capacitance of 2 µF or more is not uncommon. The OCIMU circuit is also able to deliver transient currents of up to 10 amperes. This is necessary as telecommunication ASICs can demand switching currents in excess of 5 amperes, whereas the normal quiescent currents drawn range from 0.1 to 100 µA. Furthermore the circuit requires only a minimum of easily performed calibration and delivers a well-regulated supply voltage to the DUT never leaving the DUT supply pin(s) floating. Another quality of the OCIMU is that this circuit attacks the problem of measuring the quiescent current in a hierarchical way.. The circuit is designed such that first the order of magnitude of the I_{DDQ} is determined, then only if the current is below a presettable level then an accurate measurement is performed. Otherwise the circuit is directly identified as a 'bad part', allowing the testing procedure to be speeded up. The drawbacks of the OCIMU circuit are that it can only serve as an off-chip monitor -as it cannot be easily integrated using a standard CMOS process due to its architectural concept-, that its testing speed is limited if current measurements with an accuracy of 1µA or better are desired -mainly due to the noise generated by its building blocks-, and that the circuit is highly sensible to noise present on the DUT's supply reference terminal -a high quality supply is needed with a noise level less than 1 mV_{ptp} to assure the monitor's measurement accuracy .

Aims of the invention

It is an aim of the present invention to disclose a test system for electronic circuits or devices which not only can serve for accurately measuring the quiescent supply current (I_{DDQ}) drawn by a circuit or device and for deciding whether the circuit or device is good or bad, but also can be easily adapted in function of the application with respect to the desired measurement range and the measurement accuracy.

It is another aim of the present invention to disclose a basic I_{DD} measurement system which can be used for as well on-chip built-in current monitoring as for off-chip current monitoring in a broad range of applications.

It is a further aim of the present invention to disclose a test system that can be used for engineering as well as production testing which does not affect the supply voltage of the devices or circuits under test, which provides high speed and high accurate measurements, which can be easily integrated in a standard CMOS process, which overcomes the partitioning problem associated with other built-in current monitors and which can be easily adapted in function of the application with respect to the desired measurement range and accuracy. The I_{DD} monitor of the present invention achieves these goals and can be used either as an off-chip or as an on-chip built-in current monitor, in both cases providing improved characteristics in comparison to other measurement devices.

Summary of the invention

Yet, is disclosed a test system (also called monitor circuit in the sequel) for the measurement of a supply current of an electronic circuit, comprising: a first part with control means for applying and controlling at least one voltage and one current on said circuit; a second part being fed by an input voltage and delivering a first output voltage and a first output current on a first terminal and a second output current on a second terminal, said first output voltage being essentially equal to said input voltage, said second output current being essentially proportional to said first output current being said supply current; and having a switch inbetween said first and said second part, being controlled by trigger means controlled by said first part, for turning said switch off or on whereby switching said second part in measurement mode or in bypass mode. The system can further comprise a third part with means for comparing said second output current with a reference whereby testing said circuit. The second part of the system can be fabricated as an integrated circuit by preference in a CMOS technology. Said second part can also be integrated with said electronic circuit under test on one integrated circuit. Said switch can be a compensated switch for minimising the charge transfer from said switch to said circuit.

The system of the invention can be configured as a I_{DD} measurement system which can be used for built-in current monitoring as for off-chip monitoring in a broad range of applications and for as well engineering as production testing. The system does not affect the supply voltage of the devices or circuits under test and provides high speed, high accurate measurements. The system of the invention provides improved characteristics in comparison to other comparable I_{DDQ} measurement devices. The system can be based on a CCII+ current conveyor structure and can be placed in the VDD power supply line of the device under test (DUT). The system can be used to either to decide if the

device or circuit under test is good or bad, based upon a comparison of the second output current against a given reference, or to measure accurately the current drawn by the device or circuit under test. The monitor can be made easily programmable to allow the us r to select the desired configuration in function of desired measurement range, accuracy and speed requirements in function of loading conditions.

The present invention can be used either as built-in current monitor as well as external test device which could further be integrated into existing Automated Test Equipment (ATE).

The system can be used as a built-in on-chip monitor, being integrated with the said device under test on one chip, or it can be used as an external monitor device which is not integrated with said integrated circuit. The system of the present invention can be used as well for engineering and development purposes as for production testing.

Brief Description of the drawings

Figs. 1 & 2 show two basic monitor configurations according to the preferred embodiment of the invention;
Figure 3 shows basic configurations in which the monitor can be used.
Figure 4 shows how the required compensated switch could be realised in the preferred embodiment of the invention.
Figure 5 shows an alternative for the voltage comparator used in basic configuration 2.
Figure 6 shows the adapted basic configuration with the voltage comparator replaced by the alternative shown in figure 5.
Figs. 7-11 show different alternative embodiments which could be used to make the monitor circuit programmable so that the user can adapt the operation of the circuit in function of his needs.

Detailed description of the invention

As an example of how to realise the system of the invention, two basic test configurations are detailed below which only differ in the way that the measurement signal is processed. The two basic configurations are shown in figure 1 and 2.

The system (also called monitor circuit in the sequel) of the invention comprises basically a bypass unit (1), a second generation current conveyor based measurement unit (2), a comparison/evaluation unit (3) and an optional latch unit (4) to hold the measurement result until the result of the next measurement is valid. The latch is controlled by the inverse of the signal TRIG, which controls the operation of the bypass unit, generated by the inverter (6). The two basic units differ in the way the comparison with respect to a reference is performed. In both cases the monitor circuit can be used either to compare the measured current against a predefined reference value and in that way deciding whether the circuit is good or bad or to measure accurately the current drawn by the DUT by changing the reference to which the current is compared to, to measure the reference value which makes that the comparator used changes state. Out of the value of the reference used, the actual current drawn can then be easily calculated.

The bypass unit (1) is used to deliver the transient currents to the DUT which occur when the state of the DUT is changed, this unit comprises basically of a power MOSFET with very low on resistance. To avoid charge transfer from the bypass to the DUT, which influences the measurement, when the bypass switch changes state, a compensation is required. The measurement unit measures accurately the current drawn by the DUT when the bypass is not active, without affecting the DUT's supply voltage and generates at its output a current which is directly proportional and at least equal to the current drawn by the DUT. To achieve this a second generation based current conveyor structure is used (2), consisting of a regulating opamp (or ota) (11) with high slew rate to have a short reaction time, necessary to keep the voltages on its two inputs equal in function of changing load conditions, a voltage shifting circuit (12) to avoid cross-over distortion, a pair of complementary MOS driving transistors (13,14) which deliver the current required by the DUT and a pair of either simple or regulated cascode current mirrors (15,16) to copy the current drawn by the DUT and to generate the output current of the measurement unit. The further processing of this output current Io is then function of the basic configuration used.

For the first configuration, depicted in figure 1, a high accurate current comparator (3) is used to compare the measurement value (Io) against an internal reference current (Ir). This internal reference current is inverse proportional to the externally supplied reference current (Iref) using a current mirror (5) with a mirror factor of 1/100. This to minimise the influence of variations on the external reference onto the measurement result. A latch (4) can then be used to sample the result of the comparison at the end of the measurement cycle.

For the second basic configuration, depicted in figure 2, a resistor (25) is used to convert the output current Io into a voltage. The voltage across the resistor (Vr) is then compared to an externally supplied reference voltage (Vref) using a voltage comparator (23). Again a latch (4) can then be used to sample the result of the comparison at the end of the measurement cycle. Changing the value of the resistor (25) allows to create different measurement ranges, based upon the interaction of the resistor on the operation of the current mirrors (15,16) which produce the measurement value Io.

Based upon these two basic configurations, other monitor structures can be created.

To evaluate the working principle and the operating conditions of the invention described, in a preferred embodiment of the invention, a layout of the monitor was made, processed and tested. The monitor was fabricated as an integrated circuit being processed in the Mietec 0.7µ CMOS technology. Hereafter a brief overview of the specifications of the fabricated monitor are given :

- Technology used : Mietec 0.7 µm N-well CMOS 5V.
- Monitor supply : 5V
- DUT supply : 3.3V
- Sensitivity : 50 nA.
- Accurate measurement range : 100nA to 600µA.
- Accuracy <= 10 nA for currents in the range from 50nA to 10 µA
- Maximum DUT supply voltage degradation : 100mV for transient currents of 100mA.
- Maximum supply voltage degradation during quiescent current measurement is 40mV.
- Test frequency of 1 MHz for Cload up to 200pF
- The 5V monitor supply can be disconnected if the monitor is not needed.
- A 1Ω compensated PMOS switch is used to bypass transient currents, the area of the switch is 650 x 205 μm^2.
- The monitor is able to handle huge digital ASIC circuits.
- The total area of the integrated monitor is 0.22 mm^2.

As stated above, as technology to implement the monitor circuit the MIETEC 0.7 µm CMOS process was used. The use of this technology is however no restriction for the realisation of the monitor, also other CMOS technologies known in the art can be used to implement the design. The demonstrator circuit is dedicated to measure the I_{DDQ} of DUTs which require a 3.3V supply, this however is also not a restriction for the present invention as the monitor circuit can be easily adapted or redesigned in function of different DUT supply voltages, or adapted to be able to operate for a given range of DUT supply voltages. Another advantage of the present invention is that only one monitor circuit is needed to measure the current of the device under test, irrespective of its complexity. As a result there are basically three ways in which the present invention can be used to perform its task. This is illustrated in figure 3.

A first configuration in which the monitor can be used is shown in figure 3.a.. In this configuration the monitor (42) is used as an off-chip monitor. The connection from the VDD supply from the ATE (Automated test Equipment) (41) to the VDD terminal of the DUT (43) is cut and the monitor is inserted between the ATE and the DUT. The ATE is controlling both the operation of the monitor as well as the operation of the DUT during the test process.

The second way the monitor can be used is depicted in figure 3.b. In this configuration the monitor (46) is integrated together with the functional circuitry (47) and both form the DUT (45). Again the ATE (44) controls the operation of the DUT (= monitor + functional circuitry) during the testing process.

A third way the monitor can be used is shown in figure 3.c. In this configuration the monitor (49) is integrated together with the BIST (Built-in Self Test) circuitry (50) and the functional circuitry (51) as one single chip, the DUT (48). This is the configuration of a self testable device of which the BIST circuitry controls the operation of both the monitor as well as the functional circuitry when the DUT is put in test mode. Using such an approach allows the circuit to verify as well its functional behaviour as well as its current behaviour without the need of external test circuitry.

The Bypass Unit (1)

The bypass unit (1) is used to deliver the transient currents to the DUT which occur when the state of the DUT is changed, this unit consist basically of a power MOSFET with very low on resistance. To avoid charge transfer, which influences the measurement, from the bypass to the DUT when the bypass switch changes state, a compensated switch is required. When the bypass switch is integrated together with the other monitor circuitry, a compensated switch can be realised. Figure 4 shows a possible realisation of a compensated switch, consisting of the switch transistor (60) and a dummy transistor (61) of which the source and the drain are shorted, driven by the inverse of the control signal TRIG, generated by the inverter (64) which drives the bypass transistor via the buffer formed by the inverters (62-63). The on resistance of the bypass switch should be selected in function of the maximum transient current drawn by the DUT and the voltage drop allowed during transients. However in order not to influence the reaction time of the measurement part, the maximum voltage drop during bypass should be less than 100 mV.

The Measurement Unit (2)

The measurement unit (2) measures accurately the current drawn by the DUT when the bypass is not active, without affecting the DUT's supply voltage and generates at its output a current (Io) which is directly proportional and

at least equal to the current drawn by the DUT. The further processing of this output current is then function of the basic configuration used. To achieve this a second generation based current conveyor structure is used, consisting of a regulating opamp (or ota) (11), a voltage shifting circuit (12), a pair of complementary MOS driving transistors (13,14) and a set of current mirrors (15,16).

The current mirrors (15,16)

The current mirrors (15,16) copy the current drawn by the DUT and generate the output current (Io) of the measurement unit (2). A current mirror factor of at least 1 is necessary to achieve accurate measurements. To realise these current mirrors (15,16) two possible configurations can be used. The first one is based upon the use of simple current mirrors, the second one makes use of regulated cascode current mirrors. The advantage of the use of simple current mirrors is that they have a broad working range and linear behaviour in their full operation range, independent upon temperature and loading conditions. The drawback of simple current mirrors is that the temperature variations may cause a small change in the mirror factor, however without affecting the linearity. This drawback can be overcome by using a bias current which is higher than the current drawn by the DUT, so that the current consumption of the mirrors is practically the same in measurement mode as in bypass mode. As a result the operating temperature will be independent of the current drawn by the DUT so that reliable and repeatable measurements are assured. Regulated cascode current mirrors have the advantage that due, to their self-regulating construction, they are not affected by temperature and process variations and thus provide the basis for repeatable and reliable measurements. The only drawback is that there is a lower bound for the linear operation range and that the linear operation range is temperature dependent.

The complementary MOS transistors (13,14)

The pair of complementary MOS driving transistors (13,14) is used to supply the DUT with the required current, they should be designed in such a way that they can deliver the maximum current of the measurement range to the DUT without problems.

The voltage shifting circuit (12)

The voltage shifting circuit (12) is necessary as an interface between the output of the regulating opamp (11) and the pair of complementary MOS transistors (13,14). This circuit takes care of a proper biasing of the pair of complementary MOS transistors (13,14) in order to prevent cross-over distortion which otherwise would affect the measurement results related to small currents.

The regulating opamp (11)

The basic task of the regulating opamp (11) is to maintain equal voltage values on its two input terminals, and in that way assuring a stable well know DUT supply voltage, and assuring that the DUT receives its required supply current by driving the current supplying pair of complementary CMOS transistors. To fulfil these tasks the opamp needs to have a high slew rate, typically > 300 V/µs, a short reaction time, necessary to keep the voltages on its two inputs equal in function of changing load conditions, low output noise and as the opamp is contained into a feedback loop, the overall combination of opamp (11), voltage shifting circuit (12) and pair of complementary MOS transistors (13,14) should have a phase margin of at least 70°.

The Comparison Unit.

For the first configuration, depicted in figure 1, the comparison unit consist of a current comparator (3), a current mirror (5) and an optional latch (4). A high accurate high speed current comparator (3) with a hysteresis less than 1 nA is used to compare the measurement value (Io) against an internal reference current (Ir). This internal reference current (Ir) is inverse proportional to the externally supplied reference current (Iref) using a current mirror (5) with a mirror factor of 1/100. This to minimise the influence of variations on the external reference onto the measurement result. A latch (4) can then be used to sample the result of the comparison at the end of the measurement cycle.

For the second basic configuration, depicted in figure 2, the comparison unit consist of a resistor (25), a voltage comparator (23) and an optional latch (4). The resistor (25) is used to convert the output current (Io) into a voltage (Vr). The value of the resistor (25), in combination with the output impedance of the current mirror (15,16) which supplies the output current (Io) of the measurement unit (2), determines the measurement range of the I_{DDQ} monitor. The fact that by changing the value of the resistor (25) the measurement range can be adapted is one of the basic advantages

of this structure. The voltage comparator (23) compares the voltage across the resistor (Vr) to an externally supplied reference voltage (Vref). The hysteresis of the comparator (24) is one of the main factors determining the accuracy of the measurement, and also the main drawback. Therefor the hysteresis should be less than 2 mV. Again a latch (4) can then be used to sample the result of the comparison at the end of the measurement cycle. Changing the resistor value allows to create different measurement ranges, based upon the interaction of the resistor (25) on the operation of the current mirrors (15,16) which produce the measurement values.

Other configurations

General

Based upon the two basic configurations, other monitor structures can be created, basically by modifying the back-end of the measurement unit (2) and/or the comparison unit, to expand the working conditions or to overcome some problem situations.

Each of the basic units can be made programmable to allow the user to select the desired measurement range or measurement accuracy or to select an optimised configuration in function of loading conditions. This can be done by adding a simple control unit (80), switches (S1-Sn) and repeating some parts of the circuitry needed to built the monitor. The control (80) unit then determines the operation state of the monitor circuit. A shift register or a counter are among the possible useful structures for the control unit. By making the Pass/Fail output bi-directional no additional pins are needed to achieve this programmability.

Replacement of the voltage comparator

To overcome the accuracy limits which occur when using a voltage comparator (23) due to its hysteresis, the configuration of basic structure 2 can be changed by replacing the voltage comparator (23) by a unit (70) consisting of a current comparator (75) , the latter preceded by a measurement unit (72) as shown in figure 5. The measurement unit should make use of regulated cascode current mirrors (73,74), to assure independence of temperature and process parameters. At it X terminal a resistor (71), with the same value of the one (25) already connected to the output of the first measurement unit (2) and thus also to the Y terminal of the second measurement unit (70), should be connected. To assure accurate measurements the actual value of the resistors (25,71) used is off less importance than the fact that they should have equal values not to introduce additional errors. Taking this fact into account would allow to integrate the whole monitor without problems. As the measurement unit (70) proceeding the current comparator (75) does have to drive nearly no capacitive load, replacing the voltage comparator (23) by a combination of a measurement unit (70) and a current comparator (75) will not affect the overall measurement speed of the monitor. For all monitor alternatives listed hereafter which use one or more voltage comparators, the voltage comparators therein can be replaced by a the combination of a measurement unit and a current comparator The adapted total monitor configuration is shown in figure 6.

Programmable monitor configurations

The basic configuration 1 of the monitor circuit can be made programmable, as shown in figure 7. The objective is to provide different measurement ranges. This can be done by repeating the mirror stage (CM_1-CM_N) of the current mirrors (81,82) present in the measurement part (2) and using different mirror factors. Selecting mirror factors equal or bigger than 1 allows to create different measurement ranges. The largest measurement range is obtained by using a mirror factor equal to one. Using a larger mirror factor reduces the measurement range but allows more accurate measurements in favour. To the output of each mirror stage of the current mirror of the measurement unit a current comparator (CC1-CCn) is connected, each of them supplied by its own internal reference current (Ir1-Irn), derived out of the external reference current (I_Ref) using a current mirror (83) with repeated mirror stages, each of them with the same mirror factor. To the output of each of the current comparators (CC1-CCn) a switch (S1-Sn) is connected which connects them to the input of the latch (4) and which allows to select the desired measurement range and accuracy by closing one of the switches. As only voltages are switched, the switches can be build using simple transfer gates, controlled by the additional control unit (80). The switches (Sm1-Smn) within the current mirrors (81,82) of the measurement unit (2) are optional. They can be used to reduce the current consumption of the monitor by activating only one mirror stage at a time. This feature is useful for built-in current monitors.

For the second basic monitor configuration different programmable configurations can be made. The first of these programmable configurations is shown in figure 8 and an alternative is shown in figure 9. As for basic configuration 2 the resistor (25) added to the output of the measurement part (2) determines the measurement range and the accuracy, changing the value of the resistor (25) allows to define the desired operating conditions. This can be done simply by

replacing the resistor (25) or by adding several resistors (R_1-R_N) to the output of the measurement unit (2) and using switches (S11-S1n) driven by the control unit (90) to make the proper selection. The switches (S11-S1n) can be placed either in between the output of the measurement unit (2) and the resistor (R_1-R_N) (figure 8) or in between the resistor (R_1-R_N) and the ground connection (figure 9). The switches (S11-S1n) should be designed to have a low on resistance in order not to influence the measurement accuracy.

Another alternative to basic structure 2 is to make the monitor programmable in function of desired accuracy and measurement range by using one selected resistor (25) and to design the current mirrors (81,82) present in the measurement part (2) so that they comprise several mirror stages (CM_1-CM_N) which are selectable as shown in figure 10. As in this case only voltages are switched, simple transfer gates can be used to do the switching actions. In this way non-linearity which could be caused by the switches (S11-S1n) connected to the current to voltage conversion resistors (R_1-R_N) could be avoided.

Another alternative to basic structure 2 is to make the monitor programmable in function of desired accuracy, measurement range and loading conditions by designing the current mirrors (81,82) present in the measurement part (2) so that it comprises several mirror stages (CM_1-CM_N) which are selectable and a voltage to current converting resistor (R_1-R_N) and accompanying comparator (VC1-VCn) connected to the output of each mirror stage, as shown in figure 11. By selecting a certain mirror stage (CM_1-CM_N) and the corresponding comparator (VC1-VCn) a certain monitor configuration is chosen. As in this case only voltages are switched, simple transfer gates can be used to do the switching actions.

Comparison with other test systems known in the art

The comparison to the prior art is made in function of the basic configuration used. In general the monitor circuit presented here offers improved accuracy, combined with a high speed measurement rate, capacitive load driving capability, and measurement repeatability for a wide range of operating conditions, with neglectable influence on the DUT's supply voltage.

The monitor realised according to the first basic structure, as shown in figure 1, (using a current comparator) offers a far better resolution, a much broader measurement range and a much smaller voltage drop during measurement than other comparable BIC monitors. In comparison to [Rub] the accuracy obtained for the same measurement range is 10 times better and the testing rate is independent upon the current measured. The following table compares several previously published monitor with the monitor proposed here. The comparison is done with respect to the set of the following reported features:

- → technology of implementation
- → sensitivity of the monitor
- → accurate working area
- → testing frequency
- → indication of the type of device used to sense the supply current
- → variation in power supply voltage when defective current being measured
- → number of input/output pins needed to provide the performance of the monitor
- → Total area of the monitor as indicated in the referenced publications

BIC monitor	[Mal]	[She]	[Hsu]	[Lup]	[Rub]	The preferred embodiment of the invention
Technology	2μm	2μm	No data	1.5μm	1.2μm	0.7μm
Sensitivity	No data	20μA	No data	No data	100nA	10nA
Accurate area	No data	23μA-330μA	25 μA	No data	100nA-100μA	50nA-600μA
Testing rate	No data	30 MHz	550 kHz	No data	No data	1 MHz
Sensing elem.	BJT	PN	PN	PN	Capacitor	CCII+
Variations in VDD/VSS	400mV	650mV	700mV	600mV	100mV	>40mV
Number of I/O pins	2/1	2/1	2/1	2/1	1/1	2/1
Total area	No data	8294μm²	No data	1440μm²	0.3mm²	0.22mm²

Note that „No data" indicates that the proper parameter has not been reported in the mentioned article.

In comparison to other I_{DDQ} monitor circuitry such as the QuiC-Mon [Wal] and the OCIMU [Man] also better performances are noted. The QuiC-Mon v3.2 is based on the Keating-Meyer Method and achieves measurements rates ranging from 50kHz-250kHz for load capacitances in the range of 1 to 5nF. During measurement the DUT is disconnected from the supply voltage, the resolution is 100nA and the maximum measurement range is 25μA.

In comparison, the circuit presented here maintains control over the DUT's supply voltage, offers a resolution which is 10 times better, has a much broader measurement range and has a measurement speed which is faster for the same loading conditions.

The OCIMU circuit uses a resistor as a sensing element and reaches a maximum measurement rate of 10kHz for a load capacitance of 2.2μF. The monitor has a resolution of 1μA for currents ranging from 1μA-1mA. By decreasing the measurement speed, better resolutions can be obtained for the same capacitive load. The resolution also increases with preservation of speed, for decreasing capacitive loads. In comparison to the OCIMU, for a capacitive load of 1 μF, the accuracy of the circuit presented here is 100 times better for currents in the range of 0 to 100 μA, while the measurement speed is only 2 times slower.

When the monitor circuit is realised according to the second basic configuration, as shown in figure 2, then the following comparison can be made. The proposed monitor can either be used as an on- or off-chip monitor. The monitor reaches measurement rates ranging from 50kHz-500kHz for capacitive loads ranging respectively from 3μF-1pF. Resolution and accuracy can be changed without loss of speed by changing the value of the current to voltage converting resistor and ranges from 100nA - 400nA for current ranges from 0 to 190μA (100nA resolution) or to 940μA (400nA resolution). The current to voltage conversion is linear within these current ranges. Compared to the QuiC-Mon, the circuit presented here can drive much higher capacitive loads and has a much broader measurement range, while the accuracy is comparable. In comparison to the OCIMU, the measurement speed is 8 times better for the same capacitive

loading range while the accuracy is 2.5 times better for the same measurement range. For a smaller measurement range the accuracy is even 5 times better. The desired accuracy and measurement range can be easily changed without loss off speed, and loss of capacitive driveability.

Compared to built-in current monitors, the circuit presented here can measure ranges of currents without changing the overhead of the monitor. The possible measurement ranges are much larger and the speed is either comparable or faster and does not depend upon loading conditions. The current to voltage conversion characteristics are linear, which makes it easy to calibrate the monitor.

References

[Mal] W. Maly and M. Patyra, "Built-in Current Testing", IEEE Journal of Solid State Circuits, pp. 425-428, Vol. 27, No. 3., March 1992

[She] T.L. Shen, J.C Dali and J.C. Lo, "A 2ns Detecting Time, 2µm CMOS Built-in Current Sensing Circuit", *IEEE Journal of Solid State Circuits,* Vol. 28, No. 1, 1993, pp. 72-77.

[Hsu] C. Hsue and C. Liu, "Built-in current sensor for I_{DDQ} in CMOS", *Proc. of ITC, 1993, pp. 635-641.*

[Rub] A. Rubio, E. Janssens, H. Casier, J.Figueras, D. Mateo, P. De Pauw and J. Segura, "A built-in quiescent current monitor for CMOS VLSI circuits", *Proc. of ED&TC 1995,* Paris, France, March 1995, pp. 581-585.

[Lup] E. Lupon, G. Górriz, C. Martinez and J. Figueras, "Compact BIC sensor for I_{DDQ} testing of CMOS Circuits", Electronics Letters, Vol. 29, No.9, April 1993, pp. 772-774.

[Man] H. Manhaeve et al., "An Off-chip I_{DDQ} Current Measurement Unit for Telecommunication ASICs", *Proceedings of the ITC94,* Washington D.C., USA, Oct. 1994, pp. 203-212.

[Wal]K.M. Wallquist, A.W. Righter†, and C.F. Hawkins, "A General Purpose I_{DDQ} Measurement Circuit," *International Test Conference 1993,* Paper 31.3, 1993, pp. 642-651.

Claims

1. A system for the measurement of a supply current of an electronic circuit, comprising:

   a first part with control means for applying and controlling at least one voltage and one current on said circuit ;
   a second part being fed by an input voltage and delivering a first output voltage and a first output current on a first terminal and a second output current on a second terminal, said first output voltage being essentially equal to said input voltage, said second output current being essentially proportional to said first output current being said supply current ;
   a switch in between said first and said second part, being controlled by trigger means controlled by said first part, for turning said switch off or on whereby switching said second part in measurement mode or in bypass mode.

2. The system as recited in claim 1 wherein said second part is an integrated circuit.

3. The system as recited in claim 1 wherein said second part is integrated with said electronic circuit on one integrated circuit.

4. The system as recited in claim 1 wherein said switch is a compensated switch for minimising the charge transfer from said switch to said circuit.

5. The system as recited in claim 4, wherein said compensated switch comprises a MOSFET transistor and a capacitor with a capacitance value being essentially equal to the parasitic capacitance of said MOSFET.

6. The system as recited in claim 4, wherein said compensated switch comprises a MOSFET transistor and additional circuitry for charging and decharging the parasitic capacitance of said MOSFET.

7. The system as recited in claim 1 further comprising a third part with means for comparing said second output current with a reference whereby testing said circuit.

8. The system as recited in claim 7, wherein said third part further comprises a latch for retaining the output voltage of said comparator while in bypass mode at the value achieved during measurement mode.

9. The system as recited in claim 7, further comprising means for making said second output current equal to or larger than said first output current.

10. The system as recited in claim 7, wherein said second part comprises:

an operational amplifier;
means for shifting the output voltage of said operational amplifier to another level; and
two complementary MOS transistors each being connected to one current mirror, forming two pairs of branches, the current in a first branch of one pair being larger than or equal to the current in the second branch of said pair, said output current being the difference of the currents in said first branches, the supply being the difference of the currents in said second branch.

11. The system as recited in claim 7, wherein said second part comprises:

an operational amplifier;
means for shifting the output voltage of said operational amplifier to another level; and
a plurality of complementary MOS transistors with a plurality of current mirrors being connected to said MOS transistors forming a plurality of pairs of branches, the current in one branch of one pair being proportional to the current in the other branch of said pair, said output current being the difference of the currents in said plurality of pairs of branches.

12. The system as recited in claim 11 wherein said complementary MOS transistors are determining the measurement range of said system.

13. The system as recited in claim 11 wherein said current mirrors are regulated cascode current mirrors.

14. The system as recited in claim 11 wherein said operational amplifier has a high slew rate.

15. The system as recited in claim 14 wherein said operational amplifier has a slew rate that is larger than 300 Volts per microsecond.

16. The system as recited in claim 7 wherein said means in said third part for comparing said second output current with a reference comprises a current source and a current mirror and a current comparator, the current of said current mirror being compared with said second output current.

17. The system as recited in claim 16 wherein the current of said current source is substantially larger than the current delivered by said current mirror.

18. The system as recited in claim 7 wherein said means in said third part for comparing said second output current with a reference comprise a resistor and a voltage source.

19. The system as recited in claim 18 wherein the stability of said resistor is such that the stability of the voltage over said resistor is of the order of milliVolts.

20. The system as recited in claim 18 wherein the resistance value of said resistor is such that said second output current is proportional with said supply current.

21. The system as recited in claim 7 wherein said means in said third part for comparing said second output current with a reference comprise at least two resistors, a current source, a current mirror, a current comparator, and a fourth part having a substantially similar structure to said second part of said system.

22. The system as recited in claim 21 wherein the current of said current source is substantially larger than the current delivered by said current mirror.

23. The system as recited in claim 22 wherein the first of said resistors defines a first input voltage for said fourth part, the second of said resistors being essentially identical to said first resistor and defining the first output current of said fourth part whereby the voltage over said second resistor is equal to said first input voltage, the current of said current mirror being compared with said second output current of said fourth part.

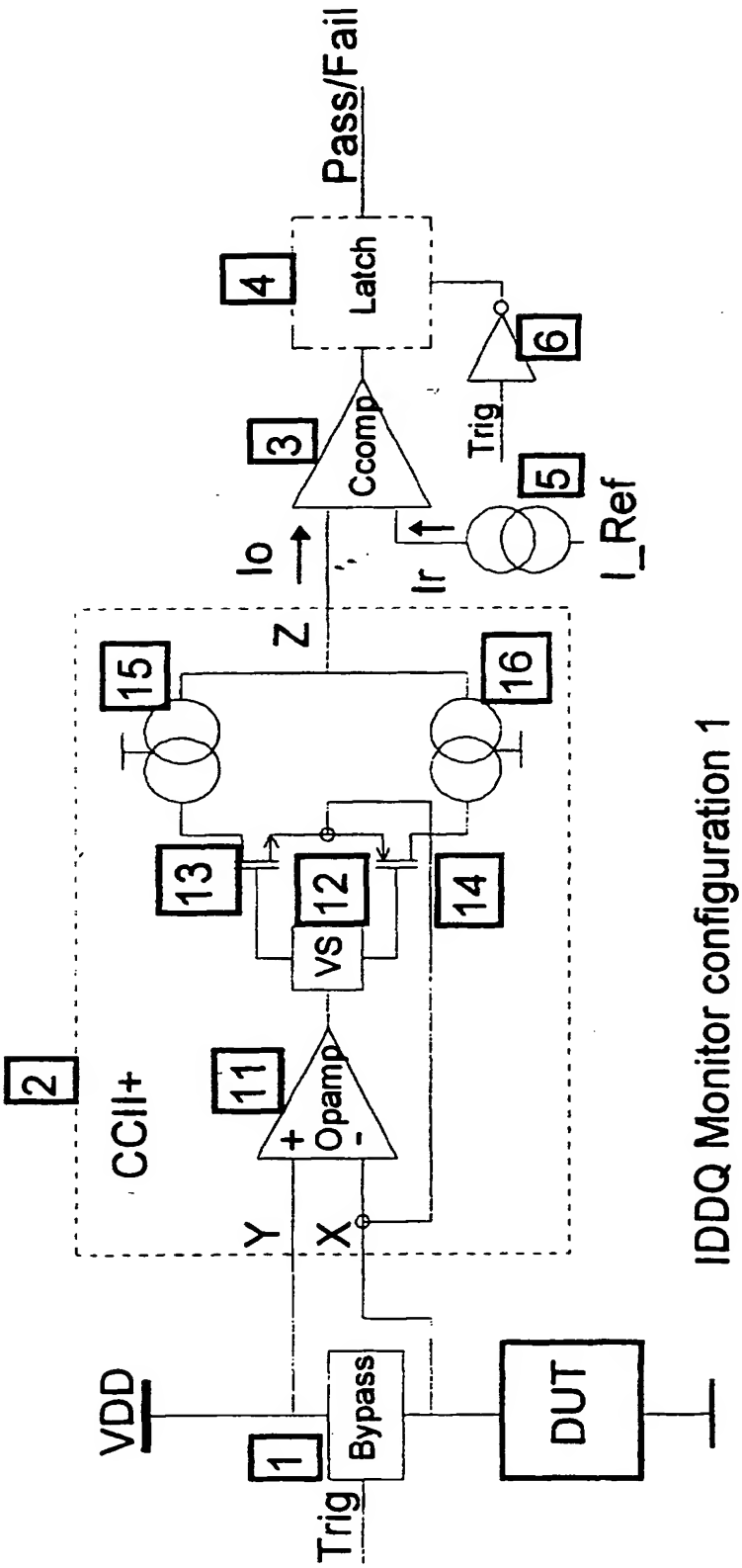


Figure 1.

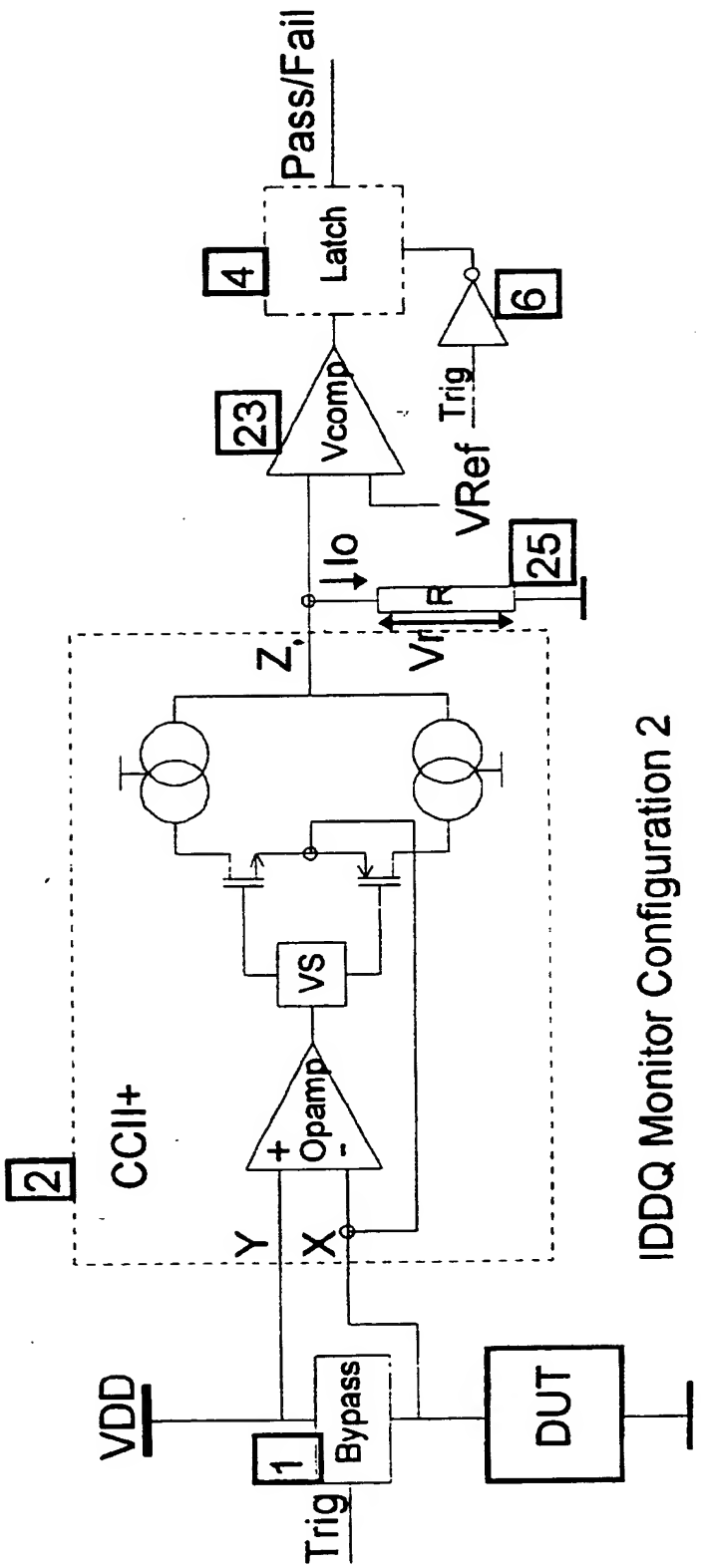


Figure 2.

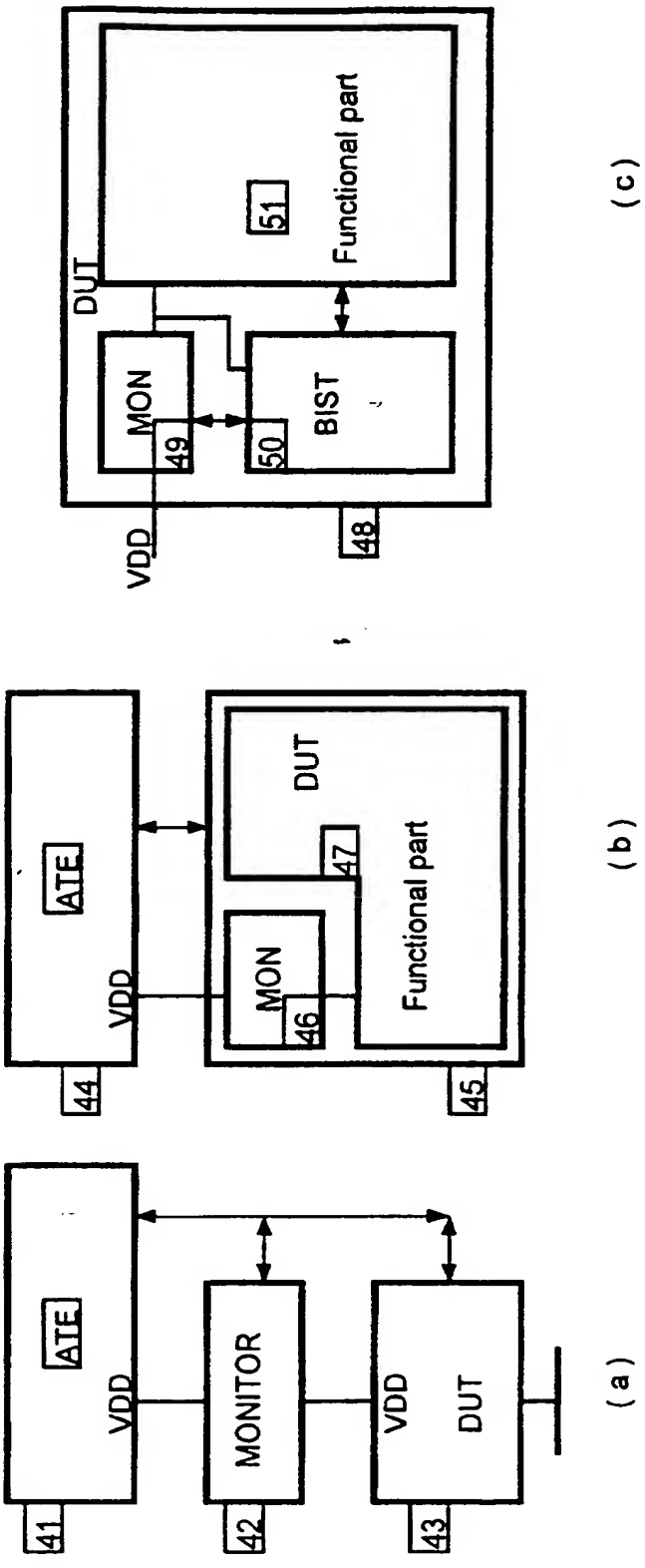


Figure 3.

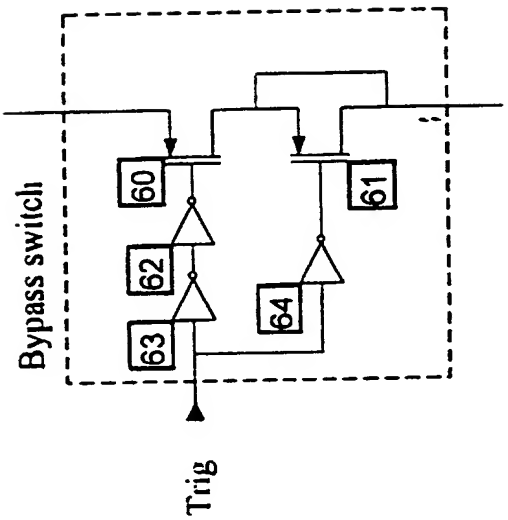


Figure 4.

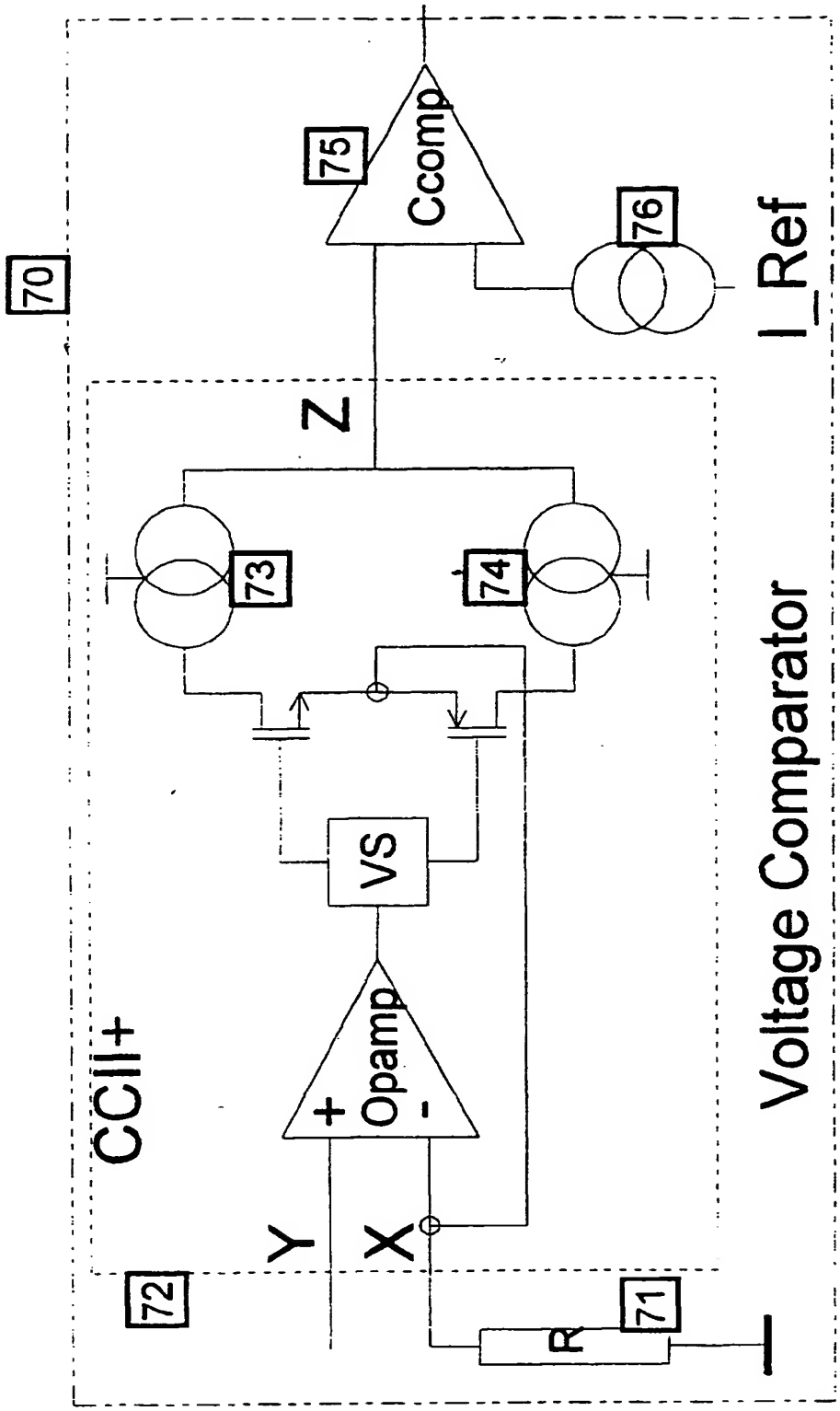


Figure 5.

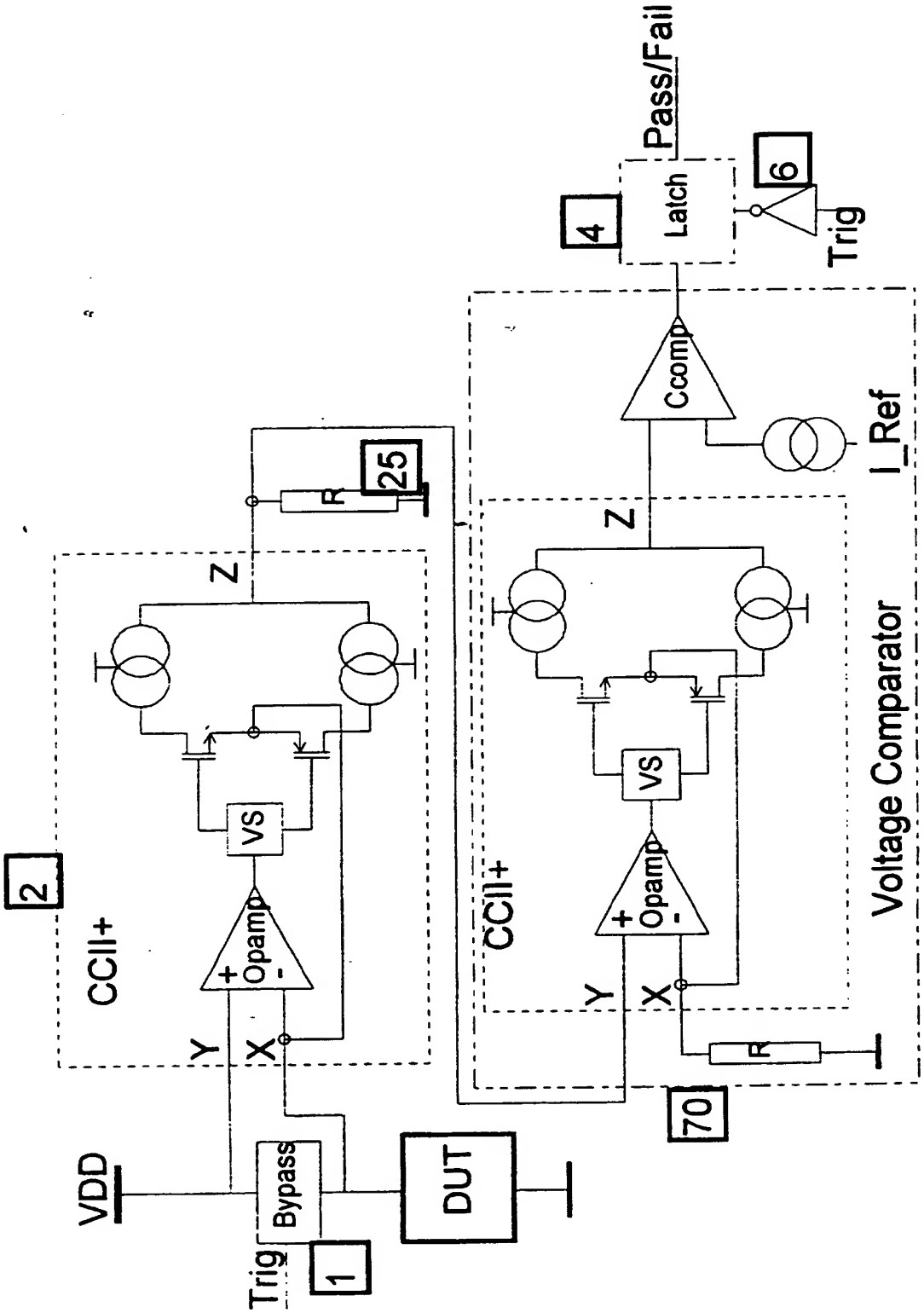


Figure 6.

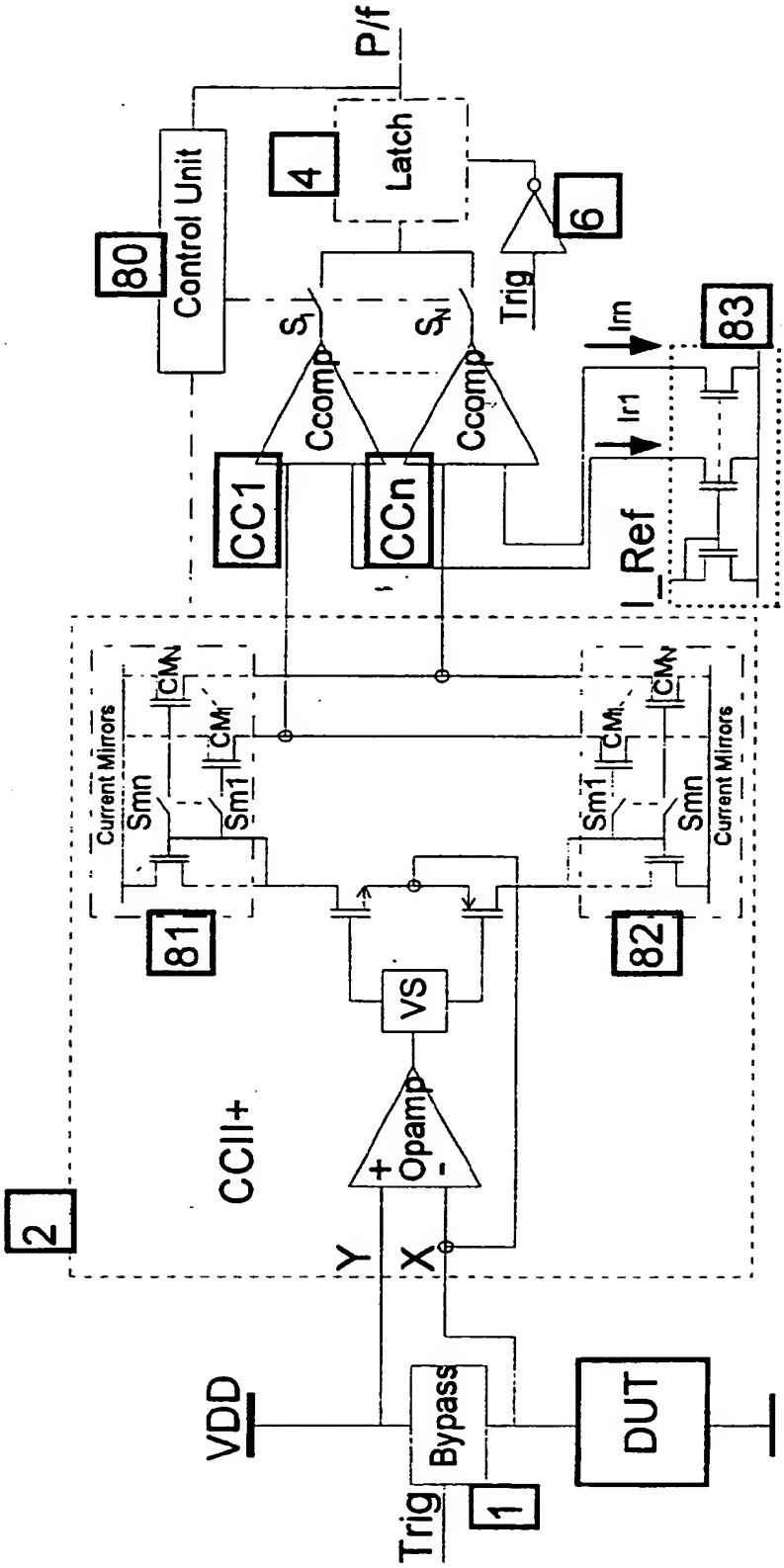


Figure 7.

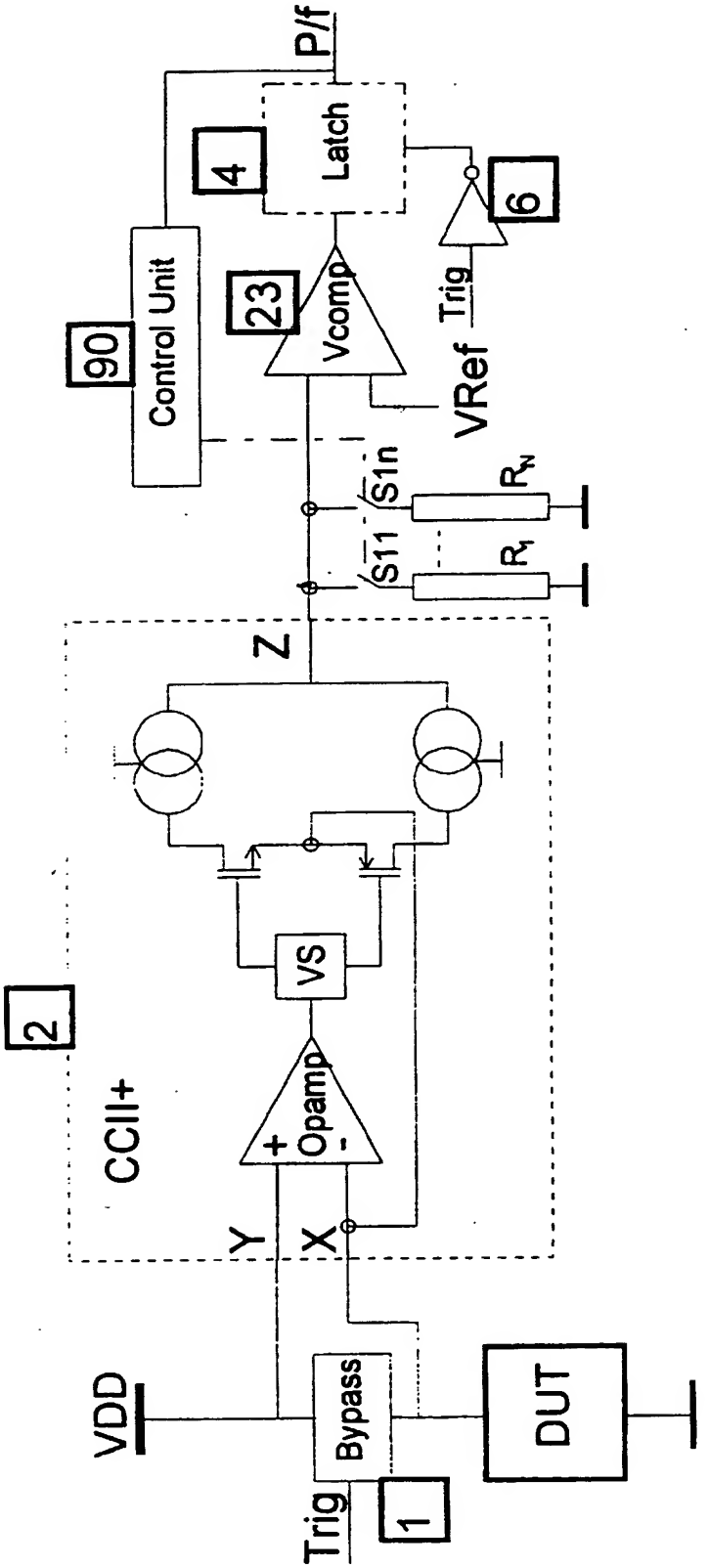


Figure 8.

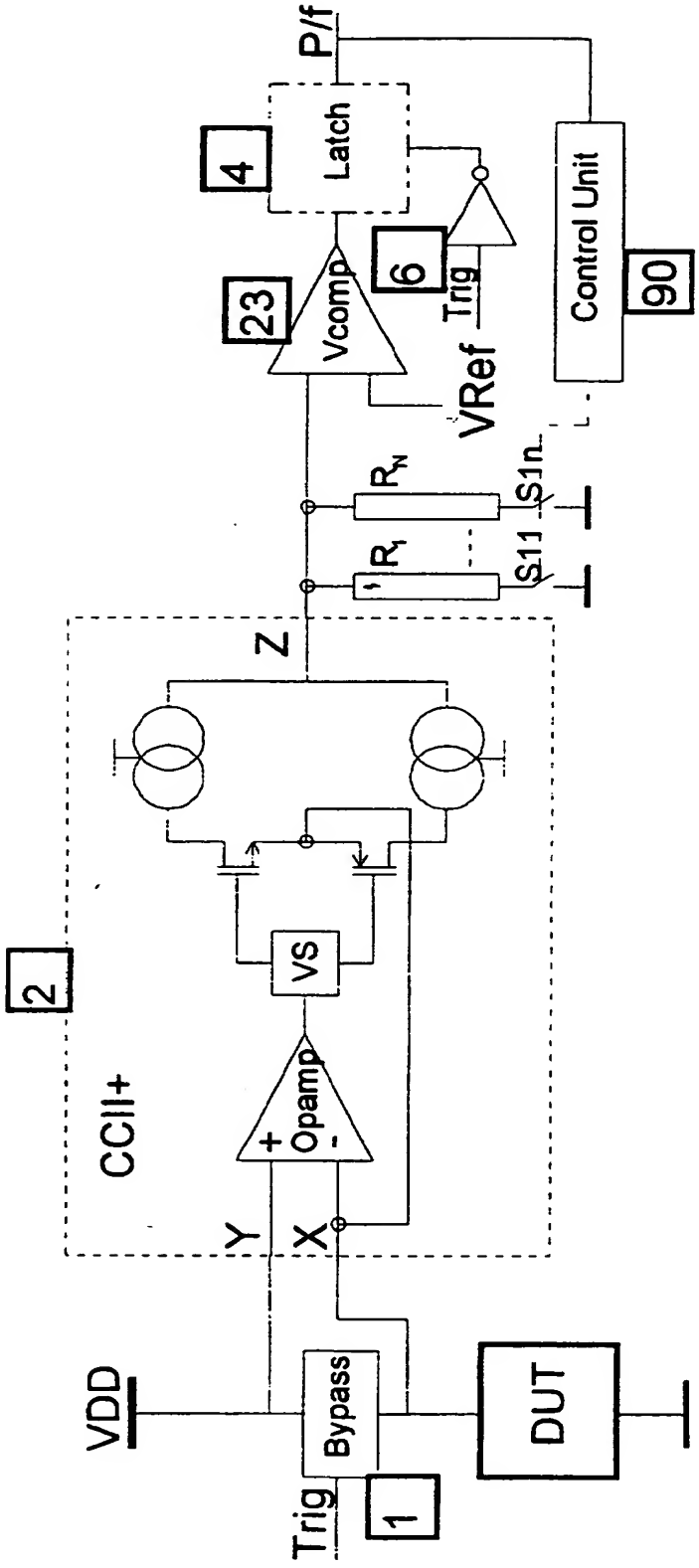


Figure 9.

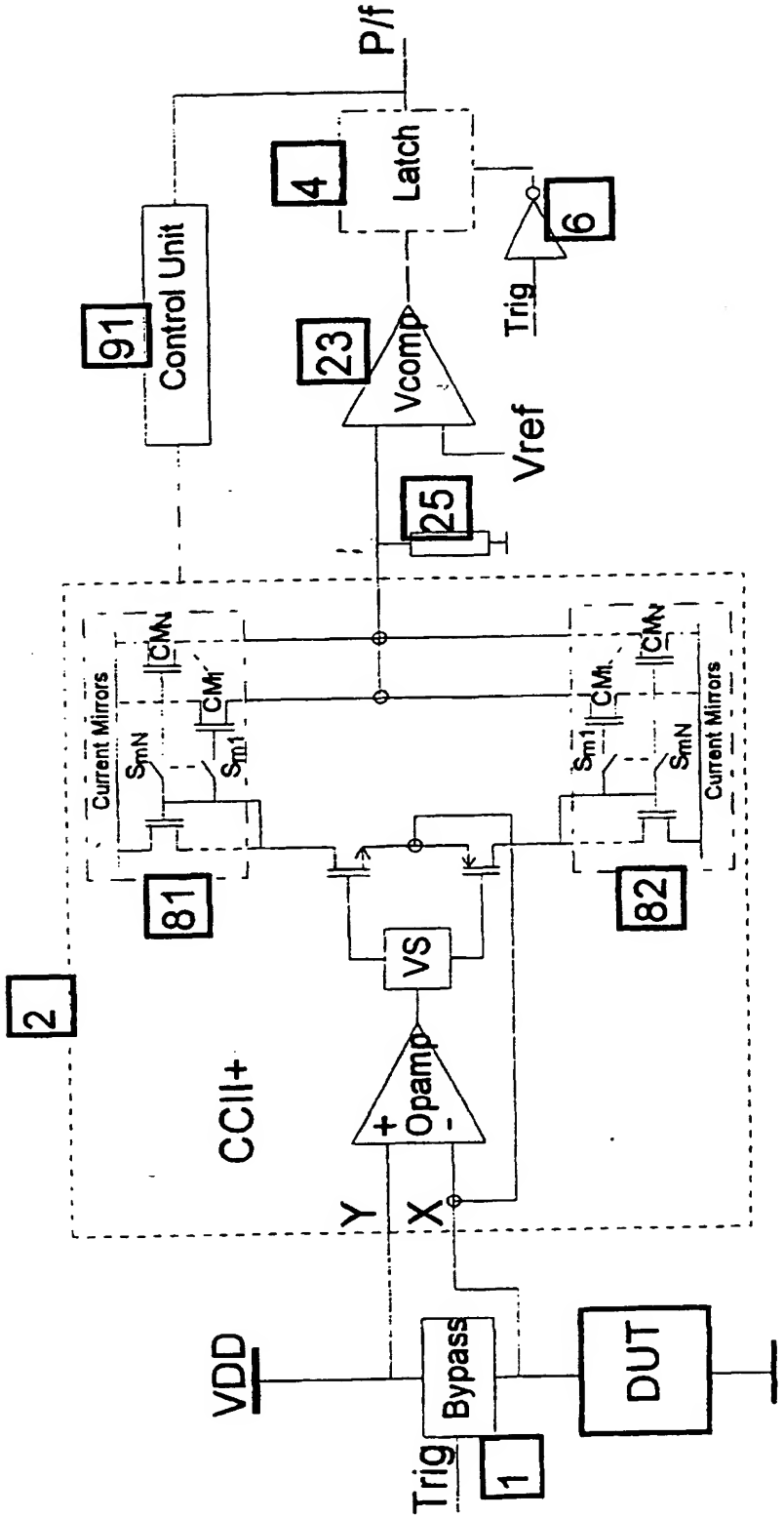


Figure 10.

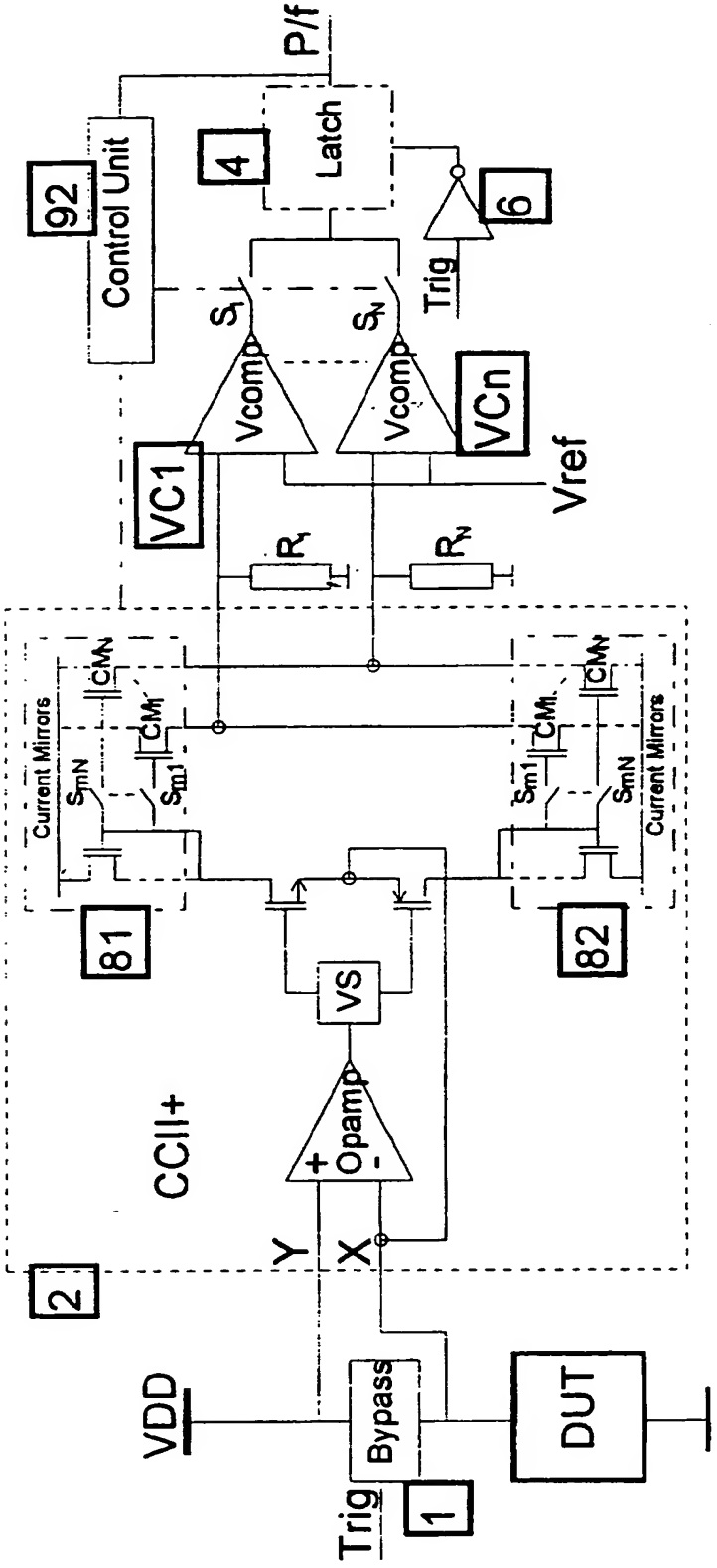

P/f
Latch
4
6
92
Control Unit
Trig
S_1
S_N
Vcomp
Vcomp
VCn
VC1
Vref
R_1
R_N
CM_N
CM_1
Current Mirrors
S_{mN}
S_{m1}
81
82
VS
Opamp
+
-
CCII+
Y
X
2
VDD
Bypass
DUT
Trig
1

Figure 11.

(19) Europäisch s Patentamt
European Patent Office
Office européen des br v ts

(11) EP 0 811 850 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
02.09.1998 Bulletin 1998/36

(43) Date of publication A2:
10.12.1997 Bulletin 1997/50

(21) Application number: **97870078.9**

(22) Date of filing: **29.05.1997**

(51) Int Cl.[6]: **G01R 31/30**, G06F 1/28, G06F 11/24

(84) Designated Contracting States:
AT BE DE ES FI FR GB IT NL SE

(30) Priority: **05.06.1996 US 19357 P**

(71) Applicants:
- **INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM VZW**
  3001 Heverlee (BE)
- **Katholieke Hogeschool Brugge-Oostende Vereniging Zonder Winstbejag**
  8000 Brugge (BE)

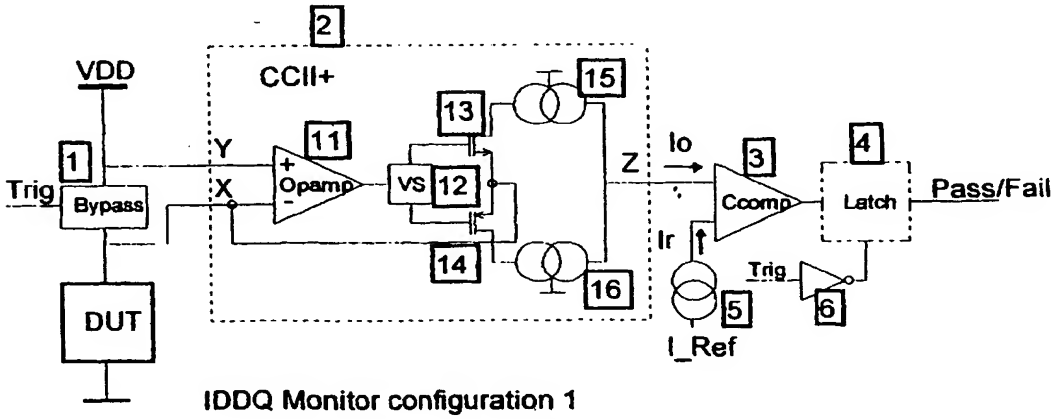
(72) Inventors:
- **Manhaeve, Hans**
  8200 Sint Michels (Brugge) (BE)
- **Kerckenaere, Stefaan**
  8480 Eernegem (BE)
- **Stopjakova, Viera**
  02962 Oravske Vesele (SK)

(74) Representative: **Van Malderen, Joelle et al**
Office Van Malderen,
Place Reine Fabiola 6/1
1083 Bruxelles (BE)

(54) High resolution supply current test system

(57) The present invention relates to a system for the measurement of a supply current of an electronic circuit, comprising:

a first part with control means for applying and controlling at least one voltage and one current on said circuit;
a second part being fed by an input voltage and delivering a first output voltage and a first output current on a first terminal and a second output current on a second terminal, said first output voltage being essentially equal to said input voltage, said second output current being essentially proportional to said first output current being said supply current;
a switch in between said first and said second part, being controlled by trigger means controlled by said first part, for turning said switch off or on whereby switching said second part in measurement mode or in bypass mode.



IDDQ Monitor configuration 1

Figure 1.

EP 0 811 850 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 87 0078

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 386 804 A (PHILIPS NV.) 12 September 1990 * abstract; figure 1A * * claims 1-13; figure 10 *	1-23	G01R31/30 G06F1/28 G06F11/24
A	JP 07 244 125 A (YOKOGAWA ELECTRIC CO.) 19 September 1995 -& US 5 608 329 A (MAKOTO I.) * abstract; claims 1-5; figures 2-4 *	1-23	
A	US 5 392 293 A (HSUE) 21 February 1995 * abstract; figure 1 *	1-23	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G06F
G11C
G01R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13 July 1998	Sarasua Garcia, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)